Amendments to the Claims

The following listing of claims replaces all prior versions, and listings, of claims in the present application.

Listing of Claims:

1-8. (Cancelled)

9. (Previously Presented) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals, wherein the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line, wherein the first and second inverters function to reduce the skew present in the complementary clock input signals; and

first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signals;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said inputs, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second, complementary internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

10. (Original) The circuit of claim 9, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

11-20. (Cancelled)

21. (Previously Presented) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second internal complementary clock signals, wherein the at least first and second complementary clock signals vary between low and high states at regular intervals and have a time lag skew relative to each other;

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor;

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor, wherein the transistors operate to output the at least first and second complementary clock signals with a reduced skew; and

first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

22. (Original) The circuit of claim 21, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

23-33. (Cancelled)

34. (Previously Presented) A circuit for reducing signal skew comprising:

at least a first and second complementary clock signal input/output line connected to receive first and second complementary clock input signals and to transmit first and second complementary clock output signals, wherein the complementary clock input signals vary between low and high states at regular intervals and have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line wherein the first and second inverters operate to reduce the skew present in the complementary clock input signals; and a first and second driver circuit, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively; and

first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

35. (Original) The circuit of claim 34, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

36-37. (Cancelled)

38. (Previously Presented) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

39. (Original) The circuit of claim 38, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

40. (Previously Presented) The circuit of claim 39, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being coupled to said inverters by the inverted enable signal.

41. (Previously Presented) The circuit of claim 40, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

42. (Previously Presented) The circuit of claim 40, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

43. (Previously Presented) The circuit of claim 40, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

44. (Previously Presented) The circuit of claim 40, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

45. (Original) The circuit of claim 38, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

46. (Original) The circuit of claim 45, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

47. (Previously Presented) The circuit of claim 46, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

48. (Previously Presented) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said

first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line; and

a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

49. (Original) The circuit of claim 48, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

50. (Previously Presented) The circuit of claim 49, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being coupled to said inverters by the inverted enable signal.

51. (Previously Presented) The circuit of claim 50, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

52. (Previously Presented) The circuit of claim 50, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

53. (Previously Presented) The circuit of claim 50, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

54. (Previously Presented) The circuit of claim 50, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

55. (Original) The circuit of claim 48, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

56. (Previously Presented) The circuit of claim 55, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

57-98. (Cancelled)